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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,957	09/08/2003	James M. Van Dyke	NVIDP033A/P000873	3047

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,957	VAN DYKE ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25* is/are allowed.

6)☒ Claim(s) *1-24,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. The related application section of the specification should reflect the current status of the parent application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 9, 11 – 13 and 15 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Novak *et al.* (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler *et al.* (US Patent No. 6,622,225, hereinafter "Kessler").

4. With respect to claims 1 and 12, Novak discloses a memory controller system (figure 1), comprising:

a memory controller (200) subsystem coupled to a plurality of computer components (30, 40, 110), the memory controller subsystem including:

at least one read or write queue (figure 2, 360) with an input coupled to one of the computer components and an output coupled to memory for queuing read or write commands to be sent to the memory, and at least one activate queue (340) with an input coupled to one of the

computer components and an output coupled to the memory for queuing activate commands to be sent to the memory;

However, Novak does not specifically disclose a plurality of memory controller subsystems. Nor does Novak disclose that the activate commands are capable of being restored to a row and a bank associated with the read or write commands at a head of the associated read or write queue. On the other hand, Kessler discloses a memory controller system that comprises a plurality of memory controller subsystems (Kessler, figure 2B 190) that are capable of restoring activate commands to a row and a bank associated with the read or write commands at a head of the associated read or write queue (Kessler, abstract, read or write memory request that results in a bank conflict is rejected and recycled through the pending request queue and eventually makes its way down to the head of the queue to generate again or "restore" the appropriate signals or commands, including those required to activate the appropriate rows and columns for memory access).

It would have been obvious to one of ordinary skill in the art, having the teachings of Kessler and Novak before him at the time the invention was made, to use the memory access bank conflict resolution teachings of the memory controller of Kessler in the memory controller of Novak, in order to increase parallelism in memory access while avoiding bank conflicts (Kessler, col. 3, lines 30 – 60).

5. With respect to claims 2 and 13, the computer components are selected from the group consisting of a central processing unit (Novak, figure 1, 30), a display refresh module, and a graphics unit.

6. With respect to claims 3, 4, 15, and 16, the memory includes synchronous dynamic random access memory (SDRAM) (figure 2, SDRAM 70).

7. With respect to claim 5, each memory controller subsystem further includes a multiplexer (figure 2, SPM 370) having inputs coupled to the outputs of the read or write queue, and activate queue, the multiplexer further including an output coupled to the memory.

8. With respect to claim 6, the read or write commands, and the activate commands of each memory controller subsystem are loaded independent of the state of the memory (figure 2, commands are loaded as per memory requests from MRA 220).

9. With respect to claim 7, the commands are loaded in at least one of the queues of each memory controller subsystem based on rows and banks of references in at least one of the queues (Novak, col. 6, line 49 – col. 7, line 25 and figures 3 and 5, primitive operations that are queued are based on whether there is a page hit or page miss which is determined by the rows and banks referenced in the past operations which are tracked in queues 365).

10. With respect to claim 8, the loading of the commands in at least one of the queues of each memory controller subsystem is delayed based on rows and banks of references in at least one of the queues (col. 10, lines 36 – 44).

11. With respect to claim 9, each read or write queue is permitted to queue commands for only a single row in each bank (all read/write commands in the queue are only for a single row in each bank).

12. With respect to claim 11, the memory controller system arbitrarily selects to unload commands from queues associated with any of the computer components (Novak, figures 2 and 3, the commands from the computer components arrive in arbitrary order and they are unloaded through SPM 370 to the memory).

13. With respect to claim 17, the delivery of the read or write commands, and activate commands from the queues to the memory is arbitrated utilizing a timer (col. 9, lines 1 – 19, see also col. 10, lines 9 – 23).

14. With respect to claim 18, the timer arbitrates the delivery of the commands to ensure that sequential commands are delivered sequentially (col. 9, lines 5 – 8).

15. With respect to claim 19, the delivery of the read or write commands, and activate commands from the queues to the memory is arbitrated based on a predetermined order (col. 9, lines 11 – 15).

16. With respect to claim 20, the delivery of at least one of the commands is arbitrated based on a bank and a row at a head of the queues (col. 9, lines 38 – 42).

17. With respect to claim 21, the delivery of at least one of the commands is arbitrated based on the read or write commands (col. 9, lines 38 – 42).

18. With respect to claim 22, the predetermined order prioritizes the computer components (the order is predetermined as shown above and memory reeusts from the computer components are prioritized in a first come first served manner).

19. With respect to claim 23, the predetermined order prioritizes the read or write commands, the activate commands (col. 9, lines 11 – 15).

20. With respect to claim 26, wherein the restoring utilizes a field in the read or write queue that contains an activate write address (Novak, figure 7).

21. With respect to claim 27, wherein the activate address is indicated by a write pointer when the activate queue is written (NxtReq_CS and NxtReq_Col, in figures 7 and 9).

22. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Novak and Kessler as applied to claim 12 above, and further in view of Dell *et al.* (US Patent Application Publication No. 2001/0000822).

Novak and Kessler disclose all of the limitation of the parent claim as discussed above. However, they do not specifically disclose that the memory includes dual data rate (DDR) memory. On the other hand, Dell discloses a method for controlling memory where the memory includes DDR (Dell, page 1, paragraph 5).

It would have been obvious to one of ordinary skill in the art, having the teachings of Novak, Kessler and Dell before him at the time the invention was made, to use the multiple memory type and the presence detection method teaching in the RAM memory system of Dell in the design of the RAM memory system of Novak, in order to provide a memory module that is more flexible in terms of its compatibility with different computer systems (Dell, page 1 paragraph 7).

23. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Kessler and further in view of Margulis (US Patent No. 6,057,862).

Novak discloses a method, comprising:

providing a memory controller subsystem capable of:

queuing read or write commands to be sent to the memory in, at least one read or write queue with an input coupled to a computer component and an output coupled to memory, and queuing activate commands to be sent to the memory in an activate queue with an input coupled to the computer component and an output coupled to the memory (figure 2), wherein the memory controller subsystems is coupled to an advanced graphics port (AGP, 40) and a central processing computer component (CPU 30).

However, Novak does not specifically disclose at least three parallel coupled memory controller subsystems. On the other hand, Kessler discloses a computer system with at least three parallel coupled memory subsystems (figures 1 and 2B, each processing node in Kessler's computing system includes at least two memory subsystems 190, and at least three processing nodes are coupled in parallel, hence at least three memory subsystems are coupled in parallel).

It would have been obvious to one of ordinary skill in the art, having the teachings of Kessler and Novak before him at the time the invention was made, to use the multiprocessor teachings of the computer system of Kessler in the computing system of Novak, in order to be able to use Novak's invention in a multiprocessor environment. One skilled in the art would also have been motivated to combine the teachings of Kessler and Novak to increase parallelism in memory access while avoiding bank conflicts (Kessler, col. 3, lines 30 – 60).

Novak and Kessler disclose all of the limitations discussed above. However, Novak and Kessler do not specifically disclose that a first one of the memory controller subsystems is coupled to a graphics unit computer component, a second one of the memory controller subsystems is coupled to a central processing computer component, and a third one of the

memory controller subsystems is coupled to a display refresh module computer component. On the other hand, Margulis discloses that AGP systems have separate buffer memory subsystems for screen refresh and drawing operations. Margulis also discloses a memory system (figures 3 and 5) that is coupled to a CPU (308, 504), a graphics unit (334, 506), and a display refresh unit (330, 508).

It would have been obvious to one of ordinary skill in the art, having the teachings of Novak, Kessler and Margulis before him at the time the invention was made, to use the enhance controller teachings of the computer system of Margulis in the computer system of Novak and Kessler, in order to allow for a common memory architecture that can be used for display memory and main memory without having inadequate bandwidth access to the common memory impair performance (col. 3, lines 4 – 7).

Claim Rejections - 35 USC § 102

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

25. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Margulis.

Margulis discloses a memory controller system (figure 5), comprising:

at least three memory controller subsystems (figure 8, 802 – 808, see also figure 9, 908 – 912) coupled to a plurality of computer components;

wherein a first one of the memory controller subsystems is only coupled to a graphics unit computer component (802), a second one of the memory controller subsystems is only coupled to a central processing computer component (804), and a third one of the memory controller subsystems is only coupled to a display refresh module computer component (806).

Allowable Subject Matter

26. Claim 24 is allowed.

Response to Arguments

27. Applicant's arguments filed September 24, 2004, have been fully considered but they are not persuasive.

Applicant alleges that the combined teaching of Novak and Kessler references does not teach or suggest the following limitations:

"activate command"; and

"restoring the activate command to a row and a bank associated with the read or write commands at a head of a read or write queue".

As to Applicant's first allegation, the active command queue 420 is clearly shown in figure 2 of Novak's disclosure. Each memory request that is queued in the pending request queue is decoded by the request decoder 310 into activate (340), precharge (350) and read/write (360) primitive commands (see col. 8, lines 34 – 65).

As to Applicant's second allegation, the Examiner notes that the claimed limitation states "wherein the activate commands are **capable** of being restored ..." This merely claims a capability and does not claim an act or a structure that actually restores. The structure disclosed by Novak, has the capability to actually issue activate commands to a row and a bank associated with the read or write commands and the same structure is capable of supporting restoration of an activate command. In addition to having the capability, Novak discloses an actual restoration of an activate command as shown in the rejection. One of the definitions of "restore" that Applicant quotes from a dictionary is "to bring back into existence or use; reestablish;". An activate command to a row and a bank is brought back into existence along with other appropriate primitive commands (i.e. precharge, read/write) when a recycled memory request gets decoded again in an attempt to access the memory again.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
November 4, 2004

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